Suraj Sarvesha Samaga

Senior Undergraduate in Electrical Engineering, IIT Bombay
surajsamaga.github.io | surajsamaga@gmail.com

Education

Indian Institute of Technology Bombay, Mumbai, India *(Jul '19 - Present)*
Bachelor of Technology in Electrical Engineering with **Honors** CGPA - **9.53/10**

Scholastic Achievements

- Among **11** out of 1000+ students to be awarded a **Change of Branch** to **Electrical Engineering** *(2020)*
- Achieved percentile score of **99.35** in JEE (Advanced) out of 241,000 candidates *(2019)*
- Secured **99.84** percentile score in JEE (Main) amongst 1,200,000 candidates *(2019)*
- Among the top **1**% in National **Chemistry** and **Math** Olympiads, selected for INChO and INMO *(2018)*
- Selected for the **KVPY** fellowship by **IISc.** and the Govt. of India by securing **All India Rank 477** *(2018)*

Key Projects

Logarithmic SAR ADC | *Bachelor's Thesis Project* *(Aug '22 - Present)*

Guide: Prof. Rajesh Zele, EE, IITB

- Ideated new design topology of Logarithmic SAR ADCs with low mismatch errors and high-dynamic-range
- Implemented logarithmic compatible SAR logic using capacitor bank in software to verify proof of concept
- Studying Cadence Rapid Adoption Kits on linear SAR-ADC to understand and adapt circuit design flow
- Working on Cadence Virtuoso to create transistor-level ADC schematic and simulate for DR, DNL and INL

Reliability in Analog Circuits | *Research Project* *(Aug '22 - Present)*

Guide: Prof. Souvik Mahapatra, EE, IITB

- Studied frequency dependence of NBTI and HCD by degrading Ring Oscillator circuits with varying stages
- Performed NBTI and HCD checks on Voltage Decoupled Sense Amplifier circuits by applying degradation per transistor using a custom Hspice-based simulation tool to compute the change in threshold voltage
- Measured degradation via a change in DC parameters of Sense Delay and Sense Voltage

Dynamic DV Checker Coverage | *Internship* *(May '22 - Jul '22)*

Texas Instruments (India) Pvt. Ltd., Bangalore, India

- Worked as a verification engineer in the C2000 team and was extended a performance-based full-time offer
- Developed and automated PoC for SystemVerilog assertion porting from dynamic to formal testbenches
- Evaluated logical coverage of ported assertions, set up Jasper FPV formal environment to check coverage

8-bit 1 GSps Segmented Current Steering DAC Design | *Course Project* *(Apr '22)*

Guide: Prof. Rajesh Zele, EE, IITB | Course: EE 719, Mixed Signal VLSI Design

- Implemented a Segmented Current Steering DAC using GPDK 45 nm technology on Cadence Virtuoso
- Designed cascode current source bias, analog unit cell and digital driver, integrated with digital decoder
- Performed Transient, Monte Carlo and FFT simulations to achieve DNL, INL < 0.1 LSB and SFDR of 50 dB
- Completed layout of analog circuitry of unit cell, performed LVS, DRC checks and post-layout extractions

OTA Design with Class B Slew Rate Boosting Circuit | *Course Project* *(Oct '21)*

Guide: Prof. Maryam Shojaei Baghini, EE, IITB | Course: EE 618, CMOS Analog VLSI Design

- Designed OTA with auxiliary class-B SR Boosting Circuit using PTM 130nm technology on Ngspice
- Built a 2-stage Pseudo class AB main amplifier with Frequency Compensation to attain a Gain of 71.7 dB, Unity Gain Frequency of 1.61 GHz and Phase Margin of 66.17°
- Attained Slew Rate of 908 V/μs, 1% settling time of 6.8 ns and 118 dB CMRR with auxiliary circuit

Other Technical Projects

VLSI Circuits | *Course Project* *(Oct '22)*

Guide: Prof. Dinesh Sharma, EE, IITB | Course: EE 671, VLSI Design

- Designed 2-input XOR gates using CMOS, CPL and CVSL styles and analyzed output characteristics
- Implemented a 16-bit Brent Kung logarithmic fast adder in VHDL and validated design using Modelsim
- Used the Dadda Reduction Algorithm to implement a 16-bit Multiply and Accumulate circuit in VHDL

CMOS Reliability | *Course Project* *(Oct '22)*

Guide: Prof. Souvik Mahapatra, EE, IITB | Course: EE 788, Advanced CMOS Logic and Flash Memory Devices

- Used Pao-Sah, Brews and Piecewise Linear models to characterize NMOS transistors, verified with TCAD
- Fabricated NMOS transistors on TCAD and analyzed short channel effects and impact of dimension scaling
- Analyzed the Voltage acceleration, Temperature activation and power-law Time dependence of NBTI by fitting stress and recovery ΔV_{Th} data with 3 composite models of Interface, Hole and Bulk Trap phenomena

TIA Design for Receiver Frontend | *Course Project* *(Apr '22)*

Guide: Prof. Joseph John, EE, IITB | Course: EE 344, Electronics Design Lab

- Designed a 3-stage closed-loop TIA with a CS JFET and 2 CE BJTs with collector-emitter feedback on a PCB
- Ensured low noise, high Gain (100 dB) and bandwidth of 2 MHz for Plastic Optical Fiber communication
- Generated pseudorandom test signal using a shift register, used an LED for Tx and PIN Photodiode for Rx

Processor Design | *Course Project* *(Apr '22)*

Guide: Prof. Virendra Singh, EE, IITB | Course: EE 739, Processor Design

- Designed datapath, control path and instruction flowcharts for 16-bit 18-instruction mini-8085 processor
- Implemented a pipelined 6-stage 16-bit RISC Processor based on Little Computer Architecture in VHDL
- Encoded 18 instructions, used data forwarding to optimize performance and mitigate control hazards

CS-LNA Design | *Course Project* *(Apr '22)*

Guide: Prof. Jayanta Mukherjee, EE, IITB | Course: EE 619, RF Microelectronics

- Designed single-ended CS-LNA using UMC 180 nm technology on Cadence Virtuoso to operate at 2.4 GHz
- Utilized an inductively degenerated cascode common source configuration to achieve a Noise Figure <0.56 dB, Gain>15 dB and linear performance with an IIP3 of 11.61 dBm

Ferroelectric FETs in Non-Volatile Memory | *Research Project* *(May '21 - Oct '21)*

Guide: Prof. Souvik Mahapatra, EE, IITB

- Explored the use of Ferroelectric FETs in Non-Volatile Memories to reduce von Neumann bottleneck
- Analysed polarization-switching and charge-trapping for computing memory window for NVMs
- Studied and simulated Preisach Model for polarization switching for MFM, MFIM and MFIS structures

Low-Light Image Enhancement | *Course Project* *(Oct '21)*

Guide: Prof. Amit Sethi, EE, IITB | Course: EE 610, Image Processing

- Implemented two methods based on retinex theory and dual-tree complex wavelet transform, and Illumination Map Estimation to enhance the visibility of images captured under low light conditions
- Compared the performance and runtime against patch-wise, central pixel value predicting CNN model

Graph Neural Networks - Depth | *Winter Internship* *(Dec '20 - Apr '21)*

Guide: Prof. Shanmuga R, CS, IIT Gandhinagar

- Studied the performance drop of GNNs with increasing depth through an extensive literature review
- Ideated multiple approaches to overcome the problems of over-smoothing and over-squashing in GNNs
- Combined the graph convolution architecture with DropEdge optimization framework to eliminate node convergence and obtained increased accuracy by depth, with a peak of 84% at a depth of 4

Teaching Experience

Coursework | *Dept. of Electrical Engineering, IITB* *(Nov '21 - Present)*

Experience gained via coursework at IITB

- Conducted Tutorial and Problem-Solving Sessions for EE 113 (Intro to EE) and EE 204 (Analog Circuits)
- Involved in writing course reviews and organizing tutorial sessions for challenging undergraduate courses

Instructor - Tinkering Bootcamp | *Learners' Space, Technical Summer School* *(Jun '21)*

Summer course organized by IITB students to increase familiarity with basic electronics for DIY projects

- Conducted theory and demo sessions for 150+ students on the use of the NodeMCU development board
- Integrated NodeMCU board with Blynk App for IoT applications and Google Assistant for voice control

Mentorship

Institute Academic Mentor | *Student Mentorship Program, IITB* *(Apr '22 - Present)*

Selected from 388 undergraduate applicants based on a rigorous procedure consisting of a statement of purpose (SoP), peer reviews and interviews

- Mentoring 12 freshmen, ensuring that they have a comfortable transition and adaptation to college life
- Acting as a single point of contact and assisting in their academic and overall development

Department Academic Mentor | *Dept. of Electrical Engineering, IITB* *(Apr '21 - Present)*

Resources Subsystem Head

- Awarded with the Special Recognition Award for exceptional service (among 2 out of 38 mentors)
- Mentored 10 sophomores on effectively managing academic and co-curricular pursuits
- Assisting 2 academically under-performing students with effective course planning and time management
- Heading a team of 21 editors to collect and document course reviews and blogs for the EE DAMP website

Technical Skills

Programming	VHDL, Verilog, Python, MATLAB, C++, Assembly, Embedded C
Softwares	Spice, Cadence Virtuoso, Sentaurus TCAD, Keil µVision, JasperGold, Quartus, LaTeX

Key Courses

Analog	Mixed Signal VLSI Design, CMOS Analog VLSI Design, RF Microelectronics
VLSI	VLSI Design, Advanced CMOS Logic and Flash Memory Devices, Nanoelectronics, Algorithmic Design of Digital Systems, Processor Design, Microprocessors
Others	Image Processing, Machine Learning, Programming for Data Science, Error Correcting Codes, Communication Systems, Mathematical Structures for Control, Control Systems

Extracurricular Activities

- An avid cyclist, earned the title of **Randonneur** under the banner of Audax Club Parisien for completing a **200km** cycling ride well within the stipulated 13.5 hours *(2015)*
- Part of the IIT Bombay contingent that finished **2nd** at the 35th **Inter IIT** Aquatics Meet, IIT Delhi *(2022)*
- Bagged **1st** place in Inter-Hostel **Swimming** and **Quizzing** Competitions at IIT Bombay *(2022)*
- Conferred with the gold medal and **Best Outgoing Student** award at Sharada Vidyalaya, Mangalore *(2017)*
- Conducted a 14-day crash course on **Pre-College Mathematics** for competitive exams at CFAL-India *(2019)*
- Participated and led high school swimming team in various **district** and **state-level** swimming meets *(2016)*
- Competed and excelled in various **inter-school Quiz Competitions** like Thomas Cook Travel Quest, Red FM Battle of Brains, Inquisitive-NITK, Technospark-17, The Hindu Quiz *(2016)*